Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-10 (canceled).

Claim 11 (previously presented): A method for determining defects in the functional behavior of a circuit, the functional behavior of the circuit including a plurality of states and a plurality of transitions between the states, the states including a current state, a plurality of next states reachable from the current state, and a reset state, the method comprising:

simulating the functional behavior of the circuit using a description of the circuit, wherein the simulating includes:

transitioning the simulation from the current state to a first next state;

transitioning the simulation from the current state to a second next state;

wherein transitioning from the current state to the second next state is performed automatically after transitioning from the current state to the first next state without entering the reset state; and

determining defects in the functional behavior of the circuit using the simulating.

Claim 12 (previously presented): The method of Claim 11, wherein the simulation is set to the current state after transitioning to the first next state.

Claim 13 (previously presented): The method of Claim 11, wherein the first transitioning is performed in response to a first test vector, and the second state transition is performed in response to a second test vector.

Claim 14 (previously presented): The method of Claim 11, wherein:

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Santa Clara, CA 95054
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FAX (408) 982-8210

said determining of defects comprises automatically flagging, during the simulating, functional behavior of the circuit in violation of a rule associated with a predetermined pattern.

Claim 15 (previously presented): The method of Claim 11, wherein:

said determining of defects comprises automatically flagging, during the simulating, functional behavior of the circuit in violation of a rule associated with a predetermined pattern.

Claim 16 (previously presented): A method, implemented in a computer, of simulating a circuit, the circuit having a reset state of simulation in response to a simulated reset signal, the method comprising:

simulating the functional behavior of said circuit in response to a first test vector, wherein prior to said act of simulating the simulation has a current state;

restoring the simulation after said simulating act to said current state, without causing the simulation to pass through said reset state;

determining at least one next state that can be reached from the current state; and

simulating the functional behavior of said circuit in response to a second test vector, after said act of automatically restoring;

wherein each of said acts of simulating, restoring, and determining is performed in said computer.

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Claim 17 (previously presented): The method of claim 16 wherein said circuit includes at least a first controller capable of performing a plurality of first state transitions, and a second controller capable of performing a plurality of second state transitions, the method further comprising:

automatically determining, during each of said acts of simulating, for each pair of a first state transition and a second state transition performed simultaneously at least once, the number of times of said simultaneous performance, said number indicating a measure of the functional testing of said description.

Claim 18 (previously presented): The method of claim 16 further comprising:

automatically applying a predetermined rule to identify said second test vector to transition from the current state to the next state, wherein the next state can be a simulated or non-simulated state.

Claim 19 (previously presented): The method of claim 16 further comprising:

automatically enumerating said state transitions; and

automatically applying a predetermined rule to identify said second test vectors, wherein said act of automatically applying uses as input to said predetermined rule at least one of said state transitions.

Claim 20 (previously presented): The method of claim 16, wherein said circuit , includes at least a first controller capable of performing a plurality of first state transitions, and a second controller capable of performing a plurality of second state transitions, the method further comprising:

automatically determining, during each of said acts of simulating, for each pair of a first state transition and a second state transition performed simultaneously at least once, the number of times of said simultaneous performance; and

automatically applying a predetermined rule to identify said second test vector; wherein said act of automatically applying uses as input to said predetermined rule at least

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one number determined by said act of automatically determining the number of times of said simultaneous performance.

Claim 21 (previously presented): The method of claim 20 further comprising:

automatically selecting a plurality of states of the controller that have not been reached from the current state.

Claim 22 (previously presented): The method of claim 16, wherein said current state is generated by simulating said circuit in response to a predetermined test vector.

Claim 23 (previously presented): The method of claim 16 wherein said circuit includes at least one asynchronous clock signal, said asynchronous clock signal having a first clock state when the simulation is in said current state, the method further comprising: setting the asynchronous clock signal to a second clock state, said second clock state being different from said first clock state; wherein said act of setting is performed prior to said act of automatically restoring, and after said act of simulating with said first test vector.

Claim 24 (previously presented): The method of claim 16, wherein the act of simulating after automatically restoring the functional behavior of said circuit in response to test vectors identified by automatically applying a predetermined rule is repeated until all test vectors have been used in the simulation.

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Claim 25 (previously presented): The method of claim 16, further comprising:

automatically restoring the simulation to a state that is different from the current state; and

transitioning the simulation from the state different from the current state to the current state by using a sequence of test vectors identified by automatically applying a predetermined rule.

Claim 26 (previously presented): The method of claim 16, wherein simulating a plurality of next states that are reachable from the current state by using different test vectors.

Claim 27 (previously presented): A method, implemented in a computer, of simulating, the method comprising:

simulating the functional behavior of a circuit in response to a first test vector in a plurality of test vectors; wherein the simulation has a current state that is a non-reset state prior to said act of simulating;

flagging, during said act of simulating, the functional behavior of said circuit in violation of a rule associated with said predetermined pattern;

restoring the simulation to said current state, said act of automatically restoring being performed after said simulating act; and

simulating the functional behavior of said circuit in response to a second test vector, after said act of automatically restoring, to produce a circuit design description;

wherein each of said acts of simulating, flagging, and restoring is performed in said computer.

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Claim 28 (previously presented): The method of claim 27 wherein said circuit includes a first controller capable of performing a plurality of first state transitions, and a

second controller capable of performing a plurality of second state transitions, the method further comprising:

automatically determining, during each of said acts of simulating, for each pair of a first state transition and a second state transition performed simultaneously at least once, the number of times of said simultaneous performance, said number indicating a measure of the functional testing of said description.

Claim 29 (previously presented): A method, implemented in a computer, for measuring the functional testing of a description of a circuit, said circuit including a first controller capable of performing a plurality of first state transitions, and a second controller capable of performing a plurality of second state transitions, the method comprising:

testing the functional behavior of said circuit with a first controller performing a first state transition simultaneous with a second controller performing a second state transition; and

determining, during said act of testing, the number of times of said simultaneous performance, said number indicating a measure of the functional testing of said description of the circuit;

wherein the act of testing and the act of determining are performed in said computer.

Claim 30 (previously presented): A method, implemented in a computer, for measuring the functional testing of a description of a circuit, said circuit including a first controller capable of performing a plurality of first state transitions, and a second controller capable of performing a plurality of second state transitions, the method comprising:

testing the functional behavior of said circuit;

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determining, during said act of testing, for each pair of a first state transition and a second state transition performed simultaneously at least once, the number of times of said simultaneous performance, said number indicating a measure of the functional testing of said description of the circuit; and

generating descriptions of additional circuits that monitor portions of the circuit that are under testing, and during simulation each additional circuit is coupled to an instance of an arrangement of circuit elements associated with a known defective behavior, wherein the additional circuits monitor signals flowing to and from the instance and generate an error message on detecting the known defective behavior;

wherein each of said acts of testing, determining and generating is performed in said computer.

Claim 31 (previously presented): A method, implemented in a computer, of searching for functional defects in a description of a circuit with at least a controller capable of transitioning between a plurality of states, the method comprising:

simulating the functional behavior of said circuit in response to a first test vector, wherein the simulation has a current state, prior to said act of simulating;

restoring the simulation after said simulating act to said current state;

determining next states including a plurality of non-simulated states that can be reached from the current state;

simulating the functional behavior of said circuit in response to a second test vector, after said act of automatically restoring; and

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generating descriptions of additional circuits that monitor portions of the circuit that are under verification, and during simulation each additional circuit is coupled to an instance of an arrangement of circuit elements associated with a known defective behavior;

wherein the acts of simulating, restoring determining and generating are performed in said computer.

Claim 32 (previously presented): The method of claim 31, wherein the additional circuits monitor signals flowing to and from the instance and generate an error message on detecting the known defective behavior.

Claim 33 (previously presented): A method, implemented in a computer, of simulating a circuit description, the method comprising:

performing a first simulation for finding defects of said circuit description in response to a first test vector, wherein said circuit description has at least a controller capable of transitioning between a plurality of states and a current state prior to said first simulation;

restoring said first simulation to said current state after said first simulation;

determining next states including a plurality of non-simulated states that are reachable from the current state; and

performing a second simulation of said circuit description in response to a second test vector, after said act of automatically restoring said first simulation, thereby facilitating a faster method of simulation;

wherein said acts of performing, restoring, and determining are all performed in said computer.

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Claim 34 (previously presented): The method of claim 33, wherein said circuit description includes at least a first controller capable of performing a plurality of first state transitions and a second controller capable of performing a plurality of second state transitions, the method further comprising:

said computer enumerating for said first simulation and for said second simulation the number of times said first state transitions and said second state transitions occur simultaneously.

Claim 35 (previously presented): The method of claim 33 further comprising:

said computer applying a predetermined rule to identify said second test vector to transition from the current state to the next state, wherein the next state is a simulated or non-simulated state.

Claim 36 (previously presented): The method of claim 33 further comprising:

said computer enumerating said first state transition and said second state transition; and

said computer applying a predetermined rule to identify said second test vector, wherein an input to said predetermined rule is at least one of said first and said second state transitions.

Claim 37 (previously presented): The method of claim 33, wherein said circuit description includes at least a first controller capable of performing a plurality of first state transitions and a second controller capable of performing a plurality of second state transitions, the method further comprising:

said computer enumerating for each of said simulating acts, the number of said first state transitions and said second state transitions occurring simultaneously; and

said computer applying a predetermined rule to identify said second test vectors, wherein an input to said predetermined rule is at least one of said first and said second state transitions.

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Claim 38 (previously presented): The method of claim 33, wherein said current state is generated by simulating said circuit description in response to a predetermined test vector.

Claim 39 (previously presented): The method of claim 33, wherein said circuit description includes at least one asynchronous clock signal, said asynchronous clock signal having a fist clock state when the simulation is in said current state, the method further comprising:

said computer setting the asynchronous clock signal to a second clock state different from said first clock state; wherein said act of setting is performed prior to said act of automatically restoring, and after said act of simulating with said first test vector.

Claim 40 (previously presented): The method of claim 33, wherein said method is repeated by said computer until all test vectors have been used in the simulation.

Claim 41 (previously presented): The method of claim 33, further comprising:

said computer restoring said second simulation to a state that is different from the current state; and

said computer transitioning the simulation from the state different from the current state to the current state by using a sequence of test vectors identified by automatically applying a predetermined rule.

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Claim 42 (previously presented): A method, implemented in a computer, of simulating a circuit description, the method comprising:

said computer converting said circuit description into a graph for finding functional defects;

said computer examining said graph for an instance of a predetermined pattern;

said computer simulating the functional behavior of said circuit description in response to a first test vector in a plurality of test vectors; wherein the simulation has a current state that is a non-reset state prior to said act of simulating;

said computer flagging, during said act of simulating, the functional behavior of said instance in violation of a rule associated with said predetermined pattern;

said computer restoring the simulation to said current state, said act of restoring being performed after said simulating act without causing the simulation to pass through a reset state; and

said computer simulating the functional behavior of said circuit in response to a second test vector, after said act of automatically restoring, to produce a circuit design description.

Claim 43 (previously presented): The method of claim 42, wherein said circuit description includes a first controller capable of performing a plurality of first state transitions, and a second controller capable of performing a plurality of second state transitions, the method further comprising:

said computer determining, during each of said acts of simulating, for each pair of a first state transition and a second state transition performed simultaneously at least once, the number of times of said simultaneous performance, said number indicating a measure of the functional testing of said description.

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Claim 44 (previously presented): A method, implemented in a computer, of simulating a circuit description, the method comprising:

performing inside said computer a first simulation of said circuit description in response to a first test vector;

said computer automatically restoring said first simulation to said current state after said first simulation;

determining inside said computer next states including a plurality of non-simulated states that are reachable from the current state; and

performing inside said computer a second simulation of said circuit description in response to a second test vector, after said act of automatically restoring said first simulation.

Claim 45 (previously presented): The method of claim 44, wherein said circuit description includes at least one controller capable of transitioning between a plurality of states and a current state prior to said first simulation.

Claim 46 (previously presented): The method of claim 44, wherein said circuit description includes at least a first controller capable of performing a plurality of first state transitions and a second controller capable of performing a plurality of second state transitions, the method further comprising:

said computer enumerating for said first simulation and for said second simulation the number of times said first state transition and said second state transition occur simultaneously.

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Claim 47 (canceled).

Claim 48 (amended): ~~The method of claim 47 further comprising:~~

A method, implemented in a computer, of simulating a circuit description, the method comprising:

performing inside a computer a first simulation of said circuit description in response to a first test vector;

said computer restoring said first simulation to a current state after said first simulation;

said computer performing a second simulation from said current state, thereby facilitating a faster method of simulation; and

said computer determining next states including a plurality of non-simulated states that are reachable from the current state.

Claim 49 (amended): ~~The method of claim 47 further comprising:~~

A method, implemented in a computer, of simulating a circuit description, the method comprising:

performing inside a computer a first simulation of said circuit description in response to a first test vector;

said computer restoring said first simulation to a current state after said first simulation;

said computer performing a second simulation from said current state, thereby facilitating a faster method of simulation; and

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the computer performing a second simulation of said circuit description in response to a second test vector, after said act of automatically restoring said first simulation.

Claim 50 (amended): ~~The method of claim 47 wherein:~~

A method, implemented in a computer, of simulating a circuit description, the method comprising:

performing inside a computer a first simulation of said circuit description in response to a first test vector;

said computer restoring said first simulation to a current state after said first simulation;

said computer performing a second simulation from said current state, thereby facilitating a faster method of simulation;

wherein said circuit description includes at least one controller capable of transitioning between a plurality of states and a current state prior to said first simulation.

Claim 51 (amended): ~~The method of claim 47 wherein:~~

A method, implemented in a computer, of simulating a circuit description, the method comprising:

performing inside a computer a first simulation of said circuit description in response to a first test vector;

said computer restoring said first simulation to a current state after said first simulation;

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said computer performing a second simulation from said current state, thereby facilitating a faster method of simulation;

wherein said circuit description includes at least a first controller capable of performing a plurality of first state transitions and a second controller capable of performing a plurality of second state transitions, the method further comprising:

wherein said computer enumerating for said first simulation and for said second simulation the number of times said first state transition and said second state transition occur simultaneously.

Claim 52 (amended): ~~The method of claim 47 being~~

A method, implemented in a computer, of simulating a circuit description, the method comprising:

performing inside a computer a first simulation of said circuit description in response to a first test vector;

said computer restoring said first simulation to a current state after said first simulation;

said computer performing a second simulation from said current state, thereby facilitating a faster method of simulation;

wherein the method is performed to produce a circuit design description.

Claim 53 (previously presented): A method, implemented in a computer, for measuring the functional testing of a description of a circuit, said circuit including a first controller capable of performing a plurality of first state transitions, and a second controller capable of performing a plurality of second state transitions, the method comprising:

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said computer generating descriptions of additional circuits to monitor portions of said circuit, and to flag behaviors of the portions if in conformance with known defective behaviors;

said computer testing the functional behavior of said circuit with a first controller performing a first state transition simultaneous with a second controller performing a second state transition; and

automatically determining, during said act of testing, the number of times of said simultaneous performance, said number indicating a measure of the functional testing of said description of the circuit.

Claim 54 (previously presented): The method according to Claim 53, wherein said known defective behaviors are specified by the user.

Claim 55 (previously presented): The method of Claim 53, wherein, during said testing, the descriptions of said additional circuits are simulated along with the description of said circuit.

Claim 56 (previously presented): The method of Claim 53, wherein at least one of the first controller and the second controller is a protocol controller.

Claim 57 (previously presented): A method of searching for functional defects in a description of a circuit with at least a controller capable of transitioning between a plurality of states, the method comprising:

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automatically generating descriptions of additional circuits to monitor portions of said circuit, and to flag behaviors of the portions if in conformance with known defective behaviors;

using a programmed computer running a simulator program to simulate the functional behavior of said circuit in response to a test vector, wherein said circuit has a current circuit state after said act of simulating;

automatically reading the current circuit state from the simulator program; and

automatically determining a plurality of non-simulated states of said controller that can be reached from the current circuit state.

Claim 58 (previously presented): The method according to Claim 57, wherein said known defective behavior is specified by the user.

Claim 59 (previously presented): The method according to Claim 57, further comprising automatically enumerating all states of said controller that can be reached from the current circuit state.

Claim 60 (previously presented): The method according to Claim 57, further comprising recording in a computer memory a subset of simulated states of said controller.

Claim 61 (previously presented): The method according to Claim 57, wherein said controller is a protocol controller.

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Claim 62 (previously presented): A method of simulating a circuit description with at least a controller capable of transitioning between a plurality of states, the method comprising:

automatically converting said circuit description into a graph;

automatically examining said graph for an instance of a predetermined pattern;

simulating the functional behavior of said circuit description in response to a first test vector in a plurality of test vectors;

automatically recording in computer memory at least one of the states reached by said controller during said simulating;

using the state recorded in said recording and a predetermined rule to automatically identify a second test vector;

simulating the functional behavior of said circuit in a response to said second test vector; and

automatically flagging, during said act of simulating, the functional behavior of said instance in violation of a rule associated with said predetermined pattern.

Claim 63 (previously presented): The method according to Claim 62, wherein the predetermined pattern is specified by the user.

Claim 64 (previously presented): A method of simulating a circuit description, the method comprising:

performing in a computer a first simulation of said circuit description in response to a first test vector to reach a current state;

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determining in a computer next states including a plurality of non-simulated states that are reachable from the current state;

performing in a computer a second simulation of said circuit description in response to a second test vector; and

automatically flagging, during said second simulation, functional behavior of said circuit in violation of a predetermined rule.

Claim 65 (previously presented): The method according to Claim 64, wherein said predetermined rule is specified by the user.

Claim 66 (previously presented): The method according to Claim 64, further comprising using a computer to automatically traverse a representation of said circuit to determine a next state that is reachable from the current state.

Claim 67 (previously presented): The method according to Claim 64, further comprising using a computer to automatically traverse a representation of said circuit backwards for a number of cycles determined by a budget measure to determine a next state that is reachable from the current state.

Claim 68 (previously presented): The method according to Claim 64, further comprising recording in a computer memory a subset of states simulated.

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Claim 69 (previously presented): A method of automatically searching for functional defects in a description of a circuit, the method comprising:

simulating the circuit using a test vector;

determining a measure of verification performed by simulation so far; and

applying a predetermined rule, using as input said measure, to identify a plurality of next states, and to identify a test vector for transitioning to at least one of said plurality of next states.

Claim 70 (previously presented): The method of Claim 69 further comprising:

simulating the circuit again, using the test vector identified during said applying.

Claim 71 (previously presented): The method of Claim 69 further comprising, during said simulating:

automatically flagging error messages of simulation defects in said circuit.

Claim 72 (previously presented): The method of Claim 71 wherein:

said automatic flagging is performed by simulation of automatically generated descriptions of additional circuits that monitor portions of said circuit .

Claim 73 (previously presented): The method of Claim 69 wherein:

said circuit contains at least a controller capable of transitioning between a plurality of states and said measure of verification identifies the states of said controller that have been reached in simulation.

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Claim 74 (previously presented): The method according to Claim 73 further comprising:

automatically enumerating all states of said controller.

Claim 75 (previously presented): The method according to Claim 73 further comprising:

recording in a computer memory a subset of simulated states of said controller.

Claim 76 (previously presented): The method of Claim 73, wherein:

said measure of verification is used to minimize repetition of simulations that have already been performed.

Claim 77 (new) The method according to Claim 73 further comprising:

using a computer to automatically traverse a representation of said circuit to determine at least one next state.

Claim 78 (previously presented): The method of Claim 73 further comprising:

automatically generating descriptions of additional circuits to monitor portions of said circuit, and to flag behaviors of the portions if in conformance with known defective behaviors.

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Claim 79 (previously presented): The method of Claim 78 wherein:

said known defective behaviors are specified by the user.